AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-11 (canceled)

12. (currently amended) A process for forming a permanently-ON MOS transistor [[(21)]] comprising the steps of:

providing a silicon well region [[(3)]] of a first conductivity type;

depositing a first insulating layer [[(2)]] over the silicon well region [[(3)]] of the first conductivity type;

removing a portion of said deposited first insulating layer;

forming a buried silicon region [[(15)]] of a second conductivity type within the silicon well region [[(3)]] of the first conductivity type, under the removed portion of said deposited first insulating layer;

depositing a second insulating layer [[(7)]] over the first insulating layer [[(2)]] and over the buried silicon region [[(15)]] of the second conductivity type;

forming a polysilicon gate region [[(8')]] over the second insulating layer; and

forming a source region [[(9')]] of the second conductivity type and a drain region [[(9')]] of the second conductivity type within the buried silicon well region [[(3)]], said source region and drain region contacting said buried silicon region [[(15)]] of the second conductivity type.

13. (currently amended) The process according to claim 12, wherein said step of forming a source region [[(9)]] of the second conductivity type and a drain region [[(9)]] of the second conductivity type within the buried silicon well region [[(3)]] is the last step of the process among the steps of claim 12 ~~in time of the steps of claim 4~~.

14. (original) The process of claim 12, wherein said first conductivity type is a P conductivity type and said second conductivity type is a N conductivity type.

15. (original) The process of claim 12, wherein said first conductivity type is a N conductivity type and said first conductivity type is a P conductivity type.

16. (original) The process of claim 12, wherein said first gate insulating layer is a first gate oxide layer and said second gate insulating layer is a second gate oxide layer.

17. (original) The process of claim 12, wherein said permanently ON transistor makes part of an EEPROM circuit.